**LAB NO 13**



**Fall 2024**

**CSE-304L Computer Organization and Architecture Lab**

Submitted by:

Name : **Hassan Zaib Jadoon**

Reg no**. : 22PWCSE2144**

ClassSection **: A**

Signature: \_\_\_\_\_\_\_\_\_\_\_\_

Submitted to:

**Dr. Amaad Khalil**

**Department of Computer Systems Engineering**

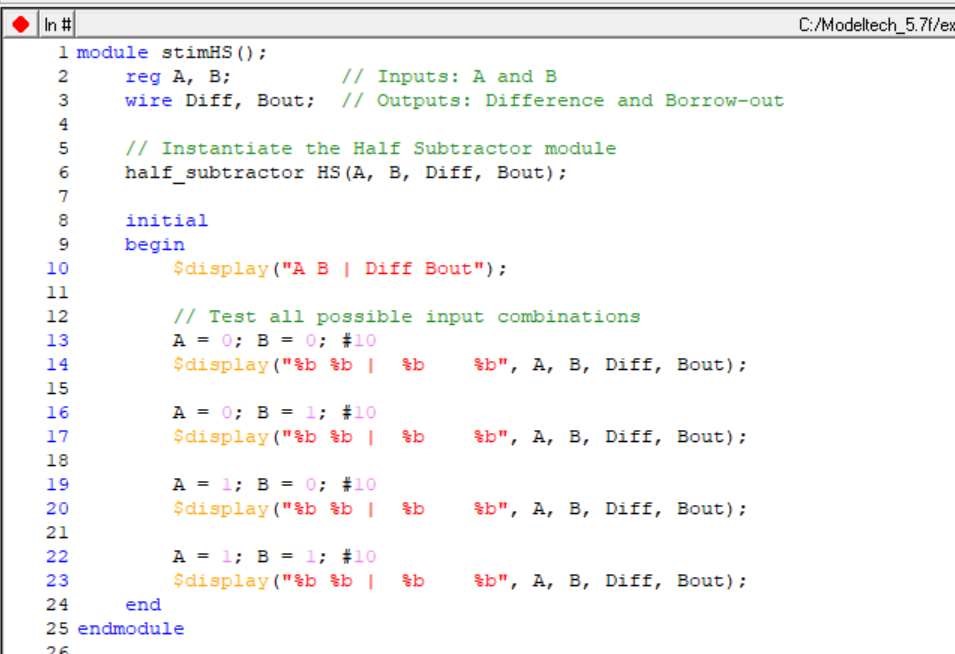
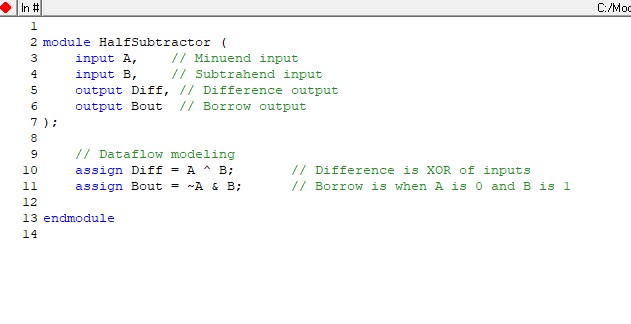
**University of Engineering and Technology, Peshawar**

**SUBTRACTOR:**

**TASK:1**

Write a Verilog code for Half Subtractor using Dataflow Level modeling.

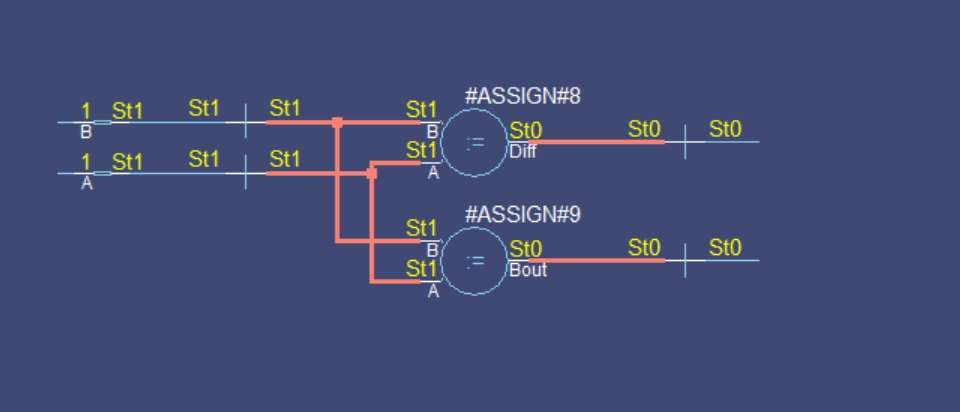
**CODE:**



**OUTPUT:**

A close-up of a white background

Description automatically generated



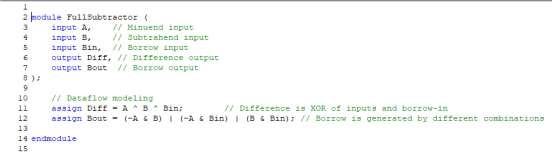
**REMARKS:**

The Verilog code for the Half Subtractor uses XOR for the Difference (A ^ B) and AND for the Borrow (~A & B), accurately modeling the subtraction logic. It's simple, clear, and efficient.

**TASK:2**

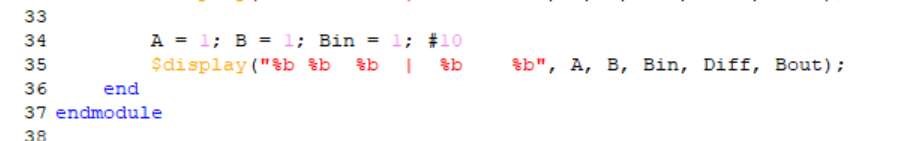
Write a Verilog code for Full Subtractor using Dataflow Level modeling.

**CODE:**



A screenshot of a computer

Description automatically generated



**OUTPUT:**

A diagram of a circuit

Description automatically generatedA screenshot of a computer

Description automatically generated

**REMARKS:**

The Verilog code for the Full Subtractor uses XOR to compute the Difference (A ^ B ^ Bin) and AND/OR operations for the Borrow (Bout). It's a compact and efficient implementation of the subtraction logic.